REMARKS/ARGUMENTS

The Applicants respectfully request reconsideration of this Application. The Applicants originally submitted Claims 1-17 in the Application. The Applicants have amended Claims 1, 7, 12, 13 and 16, and have canceled Claim 17 without prejudice of disclaimer. No claims have been added. Accordingly, Claims 1-16 are currently pending in the Application.

I. Rejection of Claims 1-9 and 12-17 under 35 U.S.C. §102

The Examiner has rejected Claims 1-9 and 12-17 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,022,787 to Ma. The Applicants respectfully assert that Ma does not anticipate Claims 1, 7 and 13 of the present Application. Specifically, Ma does not disclose a cavity formed in a second dielectric layer that exposes the first and second regions of the first conductive layer for coupling first and second leads of an integrated circuit thereto. In contrast, Ma merely discloses forming two separate cavities 134, 136 to expose opposing ends of a conductive layer.

Therefore, since Ma does not disclose the above-mentioned elements recited by independent Claims 1, 7 and 13, Ma does not anticipate these claims. In addition, since dependent Claims 2-6, 8-12 and 14-16 depend from Claims 1, 7 and 13, respectively, Ma also does not anticipate these dependent claims. Accordingly, the Applicants respectfully request the Examiner withdraw the §102 rejection with respect to Claims 1-9 and 12-16.

II. Rejection of Claims 10 and 11 under 35 U.S.C. §103

The Examiner has rejected Claims 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over Ma in view of U.S. Patent No. 5,861,322 to Caillet *et al.* (Caillet). As discussed

above, Ma fails to teach a cavity formed in a second dielectric layer exposing the first and second regions of a first conductive layer for respectively coupling first and second leads of an integrated circuit thereto, as recited by independent Claim 7. There is also no such suggestion in Ma since Ma explicitly teaches forming two separate cavities for two sidewalls that assist in forming an isolation structure for a center conductor 90. In addition, the two cavities in Ma could not be combined as a single cavity used to expose a lower metal layer since to do so would create a single sidewall that would prevent the sidewalls and upper and lower metal layers from enclosing the center conductor 90 as taught therein. In addition, Caillet does nothing to cure the deficiencies of Ma since Caillet merely teaches the formation of plated through-holes in a substrate and teaches nothing about forming a cavity in a substrate to expose two separately insulated regions of a conductive layer for attaching a lead to each of the insulated regions. As a result, the combination of Ma and Caillet do not present a *prima facie* case of obviousness of Claim 7, and, therefore, its dependant Claims 10 and 11. Accordingly, the Applicants respectfully request the Examiner withdraw the §103 rejection with respect to these claims.

The Applicants also assert that the references made of record that were not relied on also do not teach or suggest these elements. However, the Applicants reserve the right to specifically address any rejections based on these reference at such time as they are used to explicitly reject any pending claims in the present Application.

III. Conclusion

The Applicants respectfully request that the rejections be withdrawn and solicit a Notice of Allowance for Claims 1-16. The Applicants further attach hereto a marked-up version of the

amendments made to the claims. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Respectfully submitted,
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Dated: 11/22/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Claim 1 has been amended as follows:

1. (Amended) A process for manufacturing an integrated circuit package comprising:

(a) [providing] forming a substrate having a first dielectric layer, a conductive layer having a first region insulated from a second region and [formed] located above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity [exposing a portion] wherein the first and second regions are exposed within the cavity [of the conductive layer]; and

(b) interconnecting a first lead of an integrated circuit [directly] to the exposed first region [portion] and interconnecting a second lead of the integrated circuit to the exposed second region [of the conductive layer in the cavity].

(2) Claim 7 has been amended as follows:

7. (Amended) A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) [providing] forming a first dielectric layer on a substrate;

(b) [providing] forming a conductive layer having a first region insulated from a second region, above the first dielectric layer;

(c) [providing] forming a second dielectric layer above the conductive layer; and

(d) forming a cavity in the second dielectric layer to expose [a portion] the first and second regions of the conductive layer and coupling a first lead of the integrated circuit chip to the

exposed first region and coupling a second lead of the integrated circuit to the exposed second region.

(3) Claim 12 has been amended as follows:

12. (Amended) [A] The method [of manufacturing an integrated circuit package] recited in Claim 7, further comprising[:

providing the substrate of claim 7; and]

coupling the integrated circuit chip to the substrate.

(4) Claim 13 has been amended as follows:

13. (Amended) A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) [providing] forming a first dielectric layer on a substrate;

(b) [providing] forming a conductive layer having a first region insulated from a second region, above the first dielectric layer;

(c) [providing] forming a second dielectric layer above the conductive layer;

(d) [providing] forming a second conductive layer above the second dielectric layer; and

(e) forming a cavity in a first region of the second dielectric layer to expose [a portion] the first and second regions of the first conductive layer and coupling a first lead of the integrated circuit chip to the exposed first region and a second lead of the integrated circuit chip to the exposed second region.

(5) Claim 16 has been amended as follows:

16. (Amended) [A] The method [of manufacturing an integrated circuit package] recited in Claim 13, further comprising[:

providing the substrate of claim 13; and]

coupling the integrated circuit chip to the substrate.

(6) Claim 17 has been canceled without prejudice or disclaimer.